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DATE: Friday, April 09, 2004

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☐	L7	L6 same ((prior or before) near5 data near3 (chang$4 or alter$4 or modif$9 or switch$4))	1
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☐	L2	L1 same ((on adj the adj fly) or (real adj time))	41
☐	L1	(read$4 near2 output) with (convert$4 or translat$4)	4995

END OF SEARCH HISTORY

L43: Entry 6 of 15 File: USPT Feb 1, 2000

DOCUMENT-IDENTIFIER: US 6021013 A
TITLE: Timing based servo system for magnetic tape systems

Detailed Description Text (27):
The position signal noise is determined by three factors: the noise in the measurement of the transition interval times, the number of transition interval times measured per sample, and the scaling factor which converts transition interval time to position signal. The noise in the measurement of the transition interval times is governed by such factors as media noise and electronics noise and is largely independent of the pattern dimensions. The noise is considered a constant in this discussion. The number of transitions measured affects the position signal noise because of averaging. In the illustrated FIG. 9 pattern 94, four A- and B-intervals are measured per sample. In the decoder, these four measurements are averaged together to produce the position signal for the sample. Including more stripes and therefore more transitions in the pattern will lower the noise by increasing the averaging, but will also require a longer pattern, which lowers the sample rate. The scaling factor that converts transition interval time to position signal is given by the slope of the stripes.

L42: Entry 4 of 4 File: USPT Dec 14, 1982

DOCUMENT-IDENTIFIER: US 4364081 A
TITLE: Method and apparatus for processing a digital color video signal

Detailed Description Text (64):
It should be appreciated that various modifications may be effected within the scope of this invention. For example, although the above system has been explained with reference to an 8-to-10 block coding/encoding system, other block coding systems can be utilized. For example, a 3PM system in which 3-bit words are converted into 6-bit words may be utilized in which the minimum time interval between transitions of "0" and "1" bits is relatively long and the maximum time interval between transitions of "0" and "1" bits is relatively short. Thus, if the maximum time interval between transitions is 6T, when a time interval between transitions exceeds the interval 6T, the data can be considered to contain an error. Similarly, in an MFM coding system, the maximum time interval between transitions is 2T, and error detection is performed in the same manner. In addition, other than the NTSC system, the present invention is also applicable to the recording and/or reproducing of digital color video signals in a PAL system. Further, the present invention may also be utilized with a digital audio signal.

L42: Entry 1 of 4 File: USPT Sep 3, 2002

DOCUMENT-IDENTIFIER: US 6445313 B2
TITLE: Data modulating/demodulating method and apparatus for optical recording medium

Brief Summary Text (7):
The EFM method converts a one-byte or 8-bit data into a 17-bit symbol data including three-bit merging words, hereinafter referred to as "modulated data". On the other hand, the EFM+ method converts an 8-bit data into a 16-bit modulated data depending on the previous state. The modulated data is converted into a NRZI (non-return to zero inverted) code and then recorded on the optical recording medium by a mark edge method. In the data recorded on the optical recording medium in this manner, RLL (run length limited) codes, generally designated as (d, k) codes, are widely applied. Herein, d and k represent minimum and maximum run length respectively. In RLL codes, at least d "zeros" are recorded between successive data "ones", and no more than k "zeros" are recorded between successive data "ones". Since "ones" at the disc means a shift, the d constraint aims at preventing intersymbol interference. The k constraint aims at making a reproducing clock by giving a sufficient shift for a data upon reproduction. For instance, in a (2, 10) codes of DVD, there are at least two "zeros" between recorded "ones", and there are no more than ten recorded contiguous "zeros" between recorded "ones". At this time, since a data recorded is converted into the NRZI code, a minimum time interval and a maximum time interval of the recorded data are (d+1)T and (k+1)T, respectively. Herein, T represents a channel bit interval. Accordingly, in the case of a (2, 10) code, a time interval of the data recorded on the disc exists between 3T and 11T.

L32: Entry 1 of 15 File: USPT Mar 28, 2000

DOCUMENT-IDENTIFIER: US 6042249 A
TITLE: Illuminator optical assembly for an analytical instrument and methods of alignment and manufacture

Detailed Description Text (326):
The ADC 2130 inputs A0, A1 are used to select which input channel is used for the input signal. These signals are latched by a low to high transition at the CONV input. The ADC 2130 BP/UP input selects a bipolar mode if the signal is set high and a unipolar mode if the signal is set low. The ADC 2130 DRDY/ pin is a Data Ready signal that goes low at the end of the analog to digital conversion cycle, to signal to the microcontroller 2110 that data is available on the UART serial port 2119. It returns high after all bits have been shifted out or two clock cycles before new data becomes available if pin CS/ is high. The CS/ port allows access to serial port when set low. The SDATA port is a Serial data line on which data is shifted out MSB first. The SCLK port is a Serial data clock supplied by the microcontroller 2110. Preferably data changes on the falling edge of the clock. It is noted that other Nodes may utilize the internal 10 bit ADC of the Philips Model 87C597 device for digitizing data, but a different ADC may be used when greater (or less) resolution is desired, as in the HGB Node 122.

First Hit Fwd Refs

End of Result Set

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L32: Entry 15 of 15 File: USPT Oct 1, 1991

DOCUMENT-IDENTIFIER: US 5054020 A
TITLE: Apparatus for high speed data communication with asynchronous/synchronous and synchronous/asynchronous data conversion

Detailed Description Text (7):
Specifically, in byte a, a sync byte is sent. Byte b is called the DAC (Digital Access Control) byte. It carried control and status information between the converter 32 at one end of the circuit and converter 34 at the opposite end. This control information can include the baud rate, type of data (sync, async, voice, etc.) control codes for loopbacks, etc. In byte b, a DAC byte is provided with information for controlling new data before it is transmitted to the channel bank. Byte c is referred to as a "telco byte" which carries the telephone signal information between the subscriber and the channel bank.

L23: Entry 1 of 5 File: USPT Apr 23, 2002

DOCUMENT-IDENTIFIER: US 6377573 B1
TITLE: Method and apparatus for providing a minimum acceptable quality of service for a voice conversation over a data network

Abstract Text (1):
A method and apparatus for transmitting delay-sensitive data over a packet-based network involve converting the delay-sensitive data into two versions for transfer through the network with one version of the data being used to supplement the other version of the data in the event that packets are delayed or lost. In a preferred embodiment, real time voice conversation data is compressed using two different compression algorithms, where one version is more highly compressed and of a lower quality than the other. The highly compressed data is sent before corresponding packets from the less compressed data and the highly compressed packets are buffered at the receiving device to be utilized to regenerate any data segments from the less compressed packets that are lost or delayed during transmission. Sending dual versions of the same data allows the lower quality voice segment to be used as a backup in places where the high quality voice segments are lost.

Current US Cross Reference Classification (1):
370/521

L23: Entry 3 of 5 File: USPT Aug 28, 1990

DOCUMENT-IDENTIFIER: US 4953039 A
** See image for Certificate of Correction **
TITLE: Real time digital data transmission speed conversion system

Abstract Text (1):
An improved real time digital data transmission speed conversion system is disclosed which employs a method of recording high transmission rate serial format data byte groups of given density on to a recording medium. The method includes the steps of converting each high transmission rate serial format data byte group into a corresponding low transmission rate serial data byte group in real time; and, recording the lower transmission rate serial data byte groups in real time, at a density that is higher than the given density, on a moving recording medium. The system employs apparatus which include means adapted to connect the apparatus to a source of the high transmission rate serial format data byte groups of a given density; means for converting each of the serial format data byte groups into a corresponding lower transmission rate serial data byte group in real time and at a density that is higher than the given desnity; and, means adapted to connect the apparatus to a recording device for transmitting the lower transmission rate serial format data byte groups at a higher density in real time to a moving recording medium. As another feature of the system, a recording medium is provided that has digital data stored thereon in a format that includes at least two initial synchronization character bytes, followed by one or more character bytes signifying the start of a record of an event, follopwed by one or more groups of at least one byte each of data relating to the specific event, followed by one or more character bytes signifying the end of the record of the event.

Current US Original Classification (1):
360/32

Current US Cross Reference Classification (1):
360/39

L13: Entry 2 of 6 File: USPT Jun 6, 1989

DOCUMENT-IDENTIFIER: US 4837447 A
TITLE: Rasterization system for converting polygonal pattern data into a bit-map

Abstract Text (1):
A real-time rasterization system for converting plural polygonal pattern data into respective bits of a two-dimensional bit-map, wherein the respective bits of the bit-map and the locations thereof within the bit-map correspond to the shapes and locations of the polygons in a two-dimensional field and wherein the bit-map is divided into plural data stripes, each including plural scan lines having plural bits. The rasterization system converts the plural pattern data of a data stripe into plural linked data entries such that data entries which correspond to polygons intersecting the same scan line are sequentially linked, and includes a double buffer pattern data memory for storing the plural linked data entries; a processor for determining for each scan line the bits thereof intersected by each polygon represented by the respective linked data entries and for producing bit-map data corresponding to the determined bits; a double-buffer bit-map memory coupled to the processor for storing the bit-map data for each scan line of the data stripe; and a double-buffer output register for reading out sequentially the bit-map data stored in the bit-map memory.

L13: Entry 6 of 6 File: USPT Aug 12, 1975

DOCUMENT-IDENTIFIER: US 3899637 A
TITLE: Frequency shift keyed communications device

Abstract Text (1):
A full duplex frequency shift keyed communications device for bit serial transmission and reception of digital data using a communication channel comprising a two-conductor transmission line is disclosed. Each device comprises a transmitter, a receiver and a transmit/receive separator. A plurality of such devices can be commonly connected to a single communication channel wherein two such devices may communicate with each other simultaneously, or one such device may transmit while the remaining devices selectively receive the data that is transmitted. The transmitter, which includes a read-only memory and a digital to analog converter, accepts data from a real-time data processor and generates a one-cycle sinusoidal output signal in response to each transmission datum bit. If no transmission datum is available, the transmitter generates a quiescent output signal, permitting the transmission line to be used by the other devices. The transmit/receive separator cooperates with the transmission line so that the transmission line composite signal is the analog sum of the various signals being transmitted; consequently, full duplex extraction of a received signal is accomplished in the transmit/receive separator by subtracting the transmitted signal from the line conposite signal. The receiver employs a digital discrimination technique to determine the bit value corresponding to a received signal. The accuracy of the digital technique is substantially immune to phenomena such as phase distortion and oscillator frequency drift.

CLAIMS:

12. Communications apparatus according to claim 11 wherein said means for generating a transmit tone includes:

a read only memory responsive to the output signals of said counter to generate a sequence of digital output numbers in response to the predetermined sequence of oscillation counts, wherein each oscillation count causes generation of a corresponding predetermined digital output number, said read only memory having a plurality of output lines to carry output signals representative of a digital output number when such number is generated by said read only memory; and

a digital to analog converter connected to the output lines of said read only memory to generate an analog output signal having a signal level that is determined by the digital output number that is represented by the output signals of said read only memory, whereby the predetermined sequence of oscillation counts causes said digital to analog converter to generate a corresponding sequence of analog output signals comprising a transmit tone.

L13: Entry 1 of 6 File: USPT Apr 2, 2002

DOCUMENT-IDENTIFIER: US 6366687 B1
TITLE: Data converter apparatus and method particularly useful for a database-to-object inspection system

Abstract Text (1):
Data converter apparatus for converting in real time data stored in an input compact format into an output expanded real time format. The data including a plurality of groups and repetition of the groups. The groups including, each, many basic geometric figures (BGF). The data converter includes a processor adapted to selecting data relating to a predetermined division, dividing and processing the data into consecutive bins according to scan order, which bins have structural correspondence to the input format. The data converter is further capable of sub-dividing the division into sub-divisions which have structural correspondence to the output format. The data processor is further capable of processing and allocating the BGFs in the bins to sub-divisions to thereby produce a division data stream in the output expanded real time format.

Detailed Description Text (29):
Accordingly, the trapezoid data in a slice in the reference defectiess design data (which is held in "bin" representation) must be converted into a corresponding stream of pixels in the output format ready for comparison. In order to obtain the output expanded format the slice is divided into "window" representation and the BGF data in the bins are processed and allocated to the respective windows. The BGFs in the window are then transformed to sequence of lines of pixels and after undergoing so called rasterization the resulting data (which is now in the real time expanded format) is ready for comparison against the stream of pixels that originate from the inspected mask.

First Hit

Generate Collection Print

L14: Entry 6 of 95 File: JPAB Mar 22, 1984

PUB-NO: JP359049657A
DOCUMENT-IDENTIFIER: JP 59049657 A
TITLE: REAL-TIME CONVERSION SYSTEM FOR PICTURE DATA

PUBN-DATE: March 22, 1984

INVENTOR-INFORMATION:
NAME COUNTRY
MATSUBARA, YOSHITAKA
FUJIOKA, MAKOTO

US-CL-CURRENT: 702/107; 702/FOR.162
INT-CL (IPC): G06F 15/20; G01N 22/00; G01J 5/48; G01V 3/17

ABSTRACT:

PURPOSE: To process picture data which is obtained by performing conversion processing before reception and making a measurement through a dosage meter at a high speed on real-time basis, by using data for calibration obtained in the past for physical quantity conversion characteristic decision and processing.

CONSTITUTION: A physical quantity conversion table from an input/output terminal is stored in static RAMs 5-1~5-5 previously through a control part 4 before a satellite is launched. Then, the picture data from a picture data input terminal 1 is inputted in (n)-scale notation to the RAMs 5-1~5-5. At this time, only one of RAMs 5-1~5-5 stored with the physical quantity conversion table corresponding to the corresponding dosage meter is signified under the control of the control part 4 consisting of an input/output control part and an input demultiplexer. Then, (m)-bit binary data corresponding to an address is outputted from an output terminal 6 and the picture data obtained by the measurement of the dosage meter is processed at a high speed on real-time basis.

L3: Entry 1 of 14 File: USPT Jan 13, 2004

DOCUMENT-IDENTIFIER: US 6678650 B2
TITLE: Apparatus and method for converting reproducing speed

Brief Summary Text (6):
As FIG. 1 shows, the real-time speech speed converter further comprises a speech-speed converting section 5, an output-data writing section 6, an output-data storage section 7, an output-data reading section 8, and an output section 9. The speech-speed converting section 5 receives an acoustic frame signal s5 read from the data storage section 2. The speech-speed converting section 5 processes the acoustic frame signal s5 in accordance with the speech-speed converting rate s4, thereby generating an acoustic frame signal s6 that has a specific length. The acoustic frame signal s6, thus generated by the section 5. The output-data storage section 7 stores the output signal of the speech-speed converting section 5 as an acoustic frame signal s6 converted in terms of speech speed, as is illustrated in FIG. 2. The output-data writing section 6 generates a write-position signal s7 that designates the position where the signal s6 should be written in the output-data storage section 7. In the output-data storage section 7, the acoustic frame signal s6 is written at the position designated by the write-position signal s7. The output-data reading section 8 generates a read-position signal s8 that designates the position from where an output acoustic frame signal s9 should be read from the output-data storage section 7. The acoustic frame signal s9 is read from the output-data storage section 7, at the position designated by the read-position signal s8. The acoustic frame signal s9, thus read, is output through the output section 9.

L3: Entry 4 of 14 File: USPT Dec 18, 2001

DOCUMENT-IDENTIFIER: US 6331856 B1
TITLE: Video game system with coprocessor providing high speed efficient 3D graphics and digital audio signal processing

CLAIMS:

2. A method of operating a graphics display system of the type including a main processor, a coprocessor coupled to the main processor, a main random access memory coupled to the coprocessor and addressable by both the main processor and the coprocessor, and a video signal generating arrangement that produces a video signal for display, the method including the following steps:

(a) storing main processor code into the main memory;

(b) executing, with the main processor, the main processor code stored by the storing step, said executing step including storing coprocessor code, a task list, at least one texture map and a color lookup table into the main memory;

(c) fetching the task list from main memory;

(d) processing the task list with the coprocessor in accordance at least in part with the coprocessor code stored by step (b), the processing step including performing the following steps:

(1) loading the texture map and the color lookup table from the main memory into an on-chip texture memory;

(2) performing at least one 3D geometric transformation on a set of vertices using a scalar unit and a vector unit including performing multiple calculations in parallel with the vector unit;

(3) generating a triangle command based on the 3D geometric transformation;

(4) generating a pixel value in response to the triangle command;

(5) accessing the texture memory twice to provide color indexed texels based on the triangle command;

(6) combining the texels with the generated pixel value to generate a combined pixel value;

(7) accessing pixel values in a frame buffer stored in the main memory;

(8) blending the combined pixel value with at least one pixel value stored in the frame buffer;

(9) conditionally writing the combined pixel value into the frame buffer based on a comparison using a depth buffer stored in the main memory;

(10) using said scalar and vector units to generate output audio samples including

performing multiple calculations in parallel with the vector unit; and

(11) storing the output audio samples into the main memory;

(e) reading the frame buffer in real time synchronism with color television set line scanning and converting the frame buffer contents to a composite video signal; and

(f) reading the stored output audio samples in real time and converting the stored audio samples into stereo sound.

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End of Result Set

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L7: Entry 1 of 1 File: USPT Jul 10, 2001

DOCUMENT-IDENTIFIER: US 6259695 B1
TITLE: Packet telephone scheduling with common time reference

Detailed Description Text (98):
In an alternate embodiment, the operation of collection and assembly of data packets may additionally comprise the method of converting analog video signals into digital samples, prior to assembly of the digital samples into a data packet In this alternate embodiment, the scheduling also factors in the maximum additional time required to receive the converted digital samples from an analog to digital converter.

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L8: Entry 6 of 6 File: JPAB Sep 11, 1981

PUB-NO: JP356115967A
DOCUMENT-IDENTIFIER: JP 56115967 A
TITLE: SCAN CONVERTER

PUBN-DATE: September 11, 1981

INVENTOR-INFORMATION:
NAME COUNTRY
SUGANO, TOSHIO
YOKOGAWA, KAZUYOSHI
HASUMI, KANEYOSHI

ASSIGNEE-INFORMATION:
NAME COUNTRY
NIPPON ABIONIKUSU KK
NEC CORP

APPL-NO: JP55018803
APPL-DATE: February 18, 1980

INT-CL (IPC): G01S 7/12; G01S 7/44; H04N 5/02

ABSTRACT:

PURPOSE: To simply perform scan conversion in real time by preserving the maximum value of the picture signal for each picture element as well as renewing the picture signal data every time the frame or scan is changed over and providing afterglow property to the picture signal output.

CONSTITUTION: The control signal generator 1 generates the binary control signal inverted every time the frame or scan is changed over, the picture data memory 2 stores the picture data for one frame and the scan data memory 3 stores the scan data for each bit. The switch 4 compares the outputs of the control signal generator 1 and the scan data memory 3 and outputs the output signal of the multiplier 6 when one of them has H level and the other L level and at the same time, outputs the control signal to invert the scan data stored in the scan data memory 3 and outputs the picture data when both the outputs of the control signal generator 1 and the scan data memory 3 have H level or L level. The picture signal memory 2 stores the picture data having the maximum value.

L14: Entry 3 of 95 File: USPT Aug 28, 1990

US-PAT-NO: 4953039
DOCUMENT-IDENTIFIER: US 4953039 A
**** See image for Certificate of Correction ****

TITLE: Real time digital data transmission speed conversion system

DATE-ISSUED: August 28, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ploch; Louis W.	Kinnelon	NJ	07405	

US-CL-CURRENT: 360/32; 360/39, 360/48

ABSTRACT:

An improved real time digital data transmission speed conversion system is disclosed which employs a method of recording high transmission rate serial format data byte groups of given density on to a recording medium. The method includes the steps of converting each high transmission rate serial format data byte group into a corresponding low transmission rate serial data byte group in real time; and, recording the lower transmission rate serial data byte groups in real time, at a density that is higher than the given density, on a moving recording medium. The system employs apparatus which include means adapted to connect the apparatus to a source of the high transmission rate serial format data byte groups of a given density; means for converting each of the serial format data byte groups into a corresponding lower transmission rate serial data byte group in real time and at a density that is higher than the given desnity; and, means adapted to connect the apparatus to a recording device for transmitting the lower transmission rate serial format data byte groups at a higher density in real time to a moving recording medium. As another feature of the system, a recording medium is provided that has digital data stored thereon in a format that includes at least two initial synchronization character bytes, followed by one or more character bytes signifying the start of a record of an event, follopwed by one or more groups of at least one byte each of data relating to the specific event, followed by one or more character bytes signifying the end of the record of the event.

24 Claims, 14 Drawing figures
Exemplary Claim Number: 1
Number of Drawing Sheets: 8

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L39: Entry 1 of 1 File: DWPI Sep 7, 1986

DERWENT-ACC-NO: 1987-106507
DERWENT-WEEK: 198715

TITLE: System for recording data from coordinate chamber - has outputs of flip=flop register groups connected to first group inputs of asynchronous-conversion and code-delay units

INVENTOR: NIKITYUK, N M

PATENT-ASSIGNEE:

ASSIGNEE	CODE
NIKITYUK N M	NIKII

PRIORITY-DATA: 1983SU-3682753 (December 22, 1983)

Search Selected | Search ALL | Clear

PATENT-FAMILY:

	PUB-NO	PUB-DATE	LANGUAGE	PAGES	MAIN-IPC
☐	SU 1172381 A	September 7, 1986		010	

APPLICATION-DATA:

PUB-NO	APPL-DATE	APPL-NO	DESCRIPTOR
SU 1172381A	December 22, 1983	1983SU-3682753	

INT-CL (IPC): G01T 7/00

ABSTRACTED-PUB-NO: SU 1172381A
BASIC-ABSTRACT:

The system comprises n-input preamps, an n-digit register divided into n to power (1/2) groups of flip-flops and a memory. Speed of response is increased while reducing the quantity of electronic apparatus, by introducing an asynchronous-conversion and code-delay unit, together with OR-gates. A signal applied to input (1-1) sets the first group of flip-flop registers (2). The signal from this flip-flop passes via OR-gates (3-0) and (3-16) to the control input of register (2) to block the arrival of new data. The signal from the flip-flop in (2) is also applied to the async. conversion and code-delay unit (4), in company with the signal from OR-gate (3). The start signal converts the unitary code into binary code, which is applied to the input of memory (5). A sync. pulse is generated at output (9) causing the binary code to be entered. Recording then takes place only when the sync. pulse coincides with the slow-strobe pulse applied to input (11). A pulse is then generated at output (12) to reset the flip-flop group of (2-0) and a

conversion complete pulse appears at output (10) before the scheme resets for the next input.

USE - In nuclear physics, as part of electronic schemes for recording nuclear radiation and in other hodoscopic systems. Bul.33/7.9.86

CHOSEN-DRAWING: Dwg.1/2

TITLE-TERMS: SYSTEM RECORD DATA COORDINATE CHAMBER OUTPUT FLIP=FLOP REGISTER GROUP CONNECT FIRST GROUP INPUT ASYNCHRONOUS CONVERT CODE DELAY UNIT

DERWENT-CLASS: S03

EPI-CODES: S03-G;

SECONDARY-ACC-NO:
Non-CPI Secondary Accession Numbers: N1987-079806

First Hit Fwd Refs

End of Result Set

☐ Generate Collection Print

L37: Entry 1 of 1 File: USPT Jan 2, 2001

DOCUMENT-IDENTIFIER: US 6169501 B1
TITLE: Adjustable serial-to-parallel or parallel-to-serial converter

CLAIMS:

21. The method as recited in claim 19, further comprising converting a new data word in response to said conversion complete indication.

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L35: Entry 2 of 7 File: JPAB Jul 30, 1992

PUB-NO: JP404209025A
DOCUMENT-IDENTIFIER: JP 04209025 A
TITLE: CONTROL DATA CONVERTING METHOD

PUBN-DATE: July 30, 1992

INVENTOR-INFORMATION:
NAME COUNTRY
MATSUOKA, SHOGO
TAKEBE, AKIKO

ASSIGNEE-INFORMATION:
NAME COUNTRY
FUJITSU LTD

APPL-NO: JP02400301
APPL-DATE: December 4, 1990

INT-CL (IPC): G06F 9/06; G06F 9/445; G06F 9/46

ABSTRACT:

PURPOSE: To greatly shorten the stop time of a data control system by converting old data into new data by the data control system while an old program is executed, and stopping the execution of the old program at the end point of time of the conversion and executing a new program.

CONSTITUTION: A main storage device 2 and external storage devices 3-1 and 3-2 are stored with the old program PO that a central processor 1 is executing and the old data DO for executing the program. Then the device 3-2 is stored with the new program PN that the processor 1 is to execute and a data converting means 50 which converts the old data DO into the new data DN. The processor 1 executes the means 50 under the control of the program PO to convert the old data DO into the new data DN and then the new program PN is stored on the device 3-2. The processor 1 stops the execution of the old program PO temporarily, stores the new program PN and new data DN which are already stored on the device 3-2 on the device 2, and starts executing the new program PN. Consequently, the need for an on-line processing system dedicated to the data conversion is eliminated and the stop period of the system is greatly shortened.

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☐ Generate Collection | Print

L35: Entry 5 of 7 File: JPAB Nov 21, 1989

PUB-NO: JP401288735A
DOCUMENT-IDENTIFIER: JP 01288735 A
TITLE: MULTI-SPLIT PHOTOMETRY APPARATUS

PUBN-DATE: November 21, 1989

INVENTOR-INFORMATION:
NAME COUNTRY
SERITA, YASUAKI

ASSIGNEE-INFORMATION:
NAME COUNTRY
MINOLTA CAMERA CO LTD

APPL-NO: JP63119764
APPL-DATE: May 16, 1988

US-CL-CURRENT: 356/218
INT-CL (IPC): G01J 1/44

ABSTRACT:

PURPOSE: To achieve a higher efficiency of a data processing, by a method wherein an output of an A/D converter is latched temporarily by first latch circuits and a latch data is latched by second latch circuits when an A/D conversion of optoelectro transducers ends.

CONSTITUTION: First latch circuits 26~29 and second latch circuits 30~33 are arranged and data of the latch circuits 26~29 are latched by the latch circuits 30~33 when one cycle of A/D conversion of all optoelectro transducers 8~11 ends at one cycle. Thus, after the end of the A/D conversion of one set of the elements 8~11, the subsequent one set of A/D conversion can be started immediately, thereby enabling the updating to new data sequentially without a loss of time.

First Hit

End of Result Set

☐ Generate Collection | Print

L35: Entry 7 of 7 File: DWPI Sep 7, 1986

DERWENT-ACC-NO: 1987-106507
DERWENT-WEEK: 198715

TITLE: System for recording data from coordinate chamber - has outputs of flip=flop register groups connected to first group inputs of asynchronous-conversion and code-delay units

Basic Abstract Text (1):
The system comprises n-input preamps, an n-digit register divided into n to power (1/2) groups of flip-flops and a memory. Speed of response is increased while reducing the quantity of electronic apparatus, by introducing an asynchronous-conversion and code-delay unit, together with OR-gates. A signal applied to input (1-1) sets the first group of flip-flop registers (2). The signal from this flip-flop passes via OR-gates (3-0) and (3-16) to the control input of register (2) to block the arrival of new data. The signal from the flip-flop in (2) is also applied to the async. conversion and code-delay unit (4), in company with the signal from OR-gate (3). The start signal converts the unitary code into binary code, which is applied to the input of memory (5). A sync. pulse is generated at output (9) causing the binary code to be entered. Recording then takes place only when the sync. pulse coincides with the slow-strobe pulse applied to input (11). A pulse is then generated at output (12) to reset the flip-flop group of (2-0) and a conversion complete pulse appears at output (10) before the scheme resets for the next input.